## REMARKS

Applicant expresses his appreciation for the Examiner's willingness to conduct an in-office interview with Attorney Greeley and Dr. Debashis Bhattacharya on October 15, 2004, for the purpose of discussing the prior art and Applicants' current claims. Applicant explained to the Examiner via a PowerPoint Presentation that the present invention is directed to claims pertaining to a unique automated method for designing an integrated circuit design-specific cell by receiving design specification for electrical behavior or transistor-level characteristics of the design-specific cell; mapping to a transistor-level representation of the design-specific cell; and evaluating the transistor-level representation of the design-specific cell. Applicant further explained that wherein the present invention is directed to designing, mapping and evaluating a transistor-level representation of the design-specific cell, US Patent No. 6,216,252 (Dangelo et al.) is directed to a gate-level representation. In this regard Dangelo et al.'s gate-level deal with cells having Boolean expression capability, i.e., NAND, NOR, etc.). The gate-level designs or cells of Dangelo et al., are at a much higher level than the transistor-level design-specific cells according to the present invention. That is, the gate-level designs of Dangelo et al. are directed to the "NAND"/"NOR" Boolean gate level cells which by themselves include transistors. However, only the "NAND"/"NOR" Boolean gate level cells themselves may be automatically arranged by the design engineer, whereas the present invention allows the design engineer to now design, map and evaluate at the transistor-level, thereby automatically creating a new design-specific cell which heretofore did not exist. In accordance with Dangelo, Applicant clearly demonstrated that it cannot alter the transistor-level in the specific Boolean gate level cells, by optimizing the number of transistors, sizes of transistors, etc. such as that recited in the claims of the present invention.

Claims 1-38 are in the present application, wherein claims 35-38 are newly added and more specifically point out and define that the integrated circuit

design-specific cell can be selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof. Support for these new claims can be found in the Specification on Page 5, lines 16-20. Accordingly, no new matter has been introduced by these new claims.

Applicant notes with appreciation that the Examiner has indicated that claims 9, 15, 19, 25 and 29 would be allowable if placed in independent form. However, based upon the presentation during the Examiner Interview on October 15, 2004, and the remarks to follow, Applicant is of the considered opinion that all claims 1-38 are in condition for allowance.

In this regard, the outstanding Office Action objected to claims 1, 11, 21, and 30 on the basis that the phrase "design specification" as used in those claims was unclear. Applicant respectfully traverses this objection on the basis that the Specification clearly defines the phrase "design specification" and that one of ordinary skill in the art, reading the Specification, would find the phrase "design specification" to be clear and unambiguous. The design specification is specifically called out in Figure 3 as item number 125, as well as in claim 5 which specifically recited that the design specification is selected from the group consisting of: size (area), signal timing, transistor sizing, number of transistors, power consumption, length of interconnects within said design-specific cell, output signal strength, input signal impedance, noise characteristics, and a combination thereof. Accordingly, Applicant respectfully requests that this objection be withdrawn.

Applicant respectfully traverses the rejection of claims 1-8, 10-14, 16-18, 20-24, 26-28, and 30-34 under 35 USC §102(e) as being unpatentable over U.S. Patent No. 6,216,252 (Dangelo et al.). As pointed out in the Interview held on October 15, 2004, Dangelo et al. relates to "NAND"/"NOR" Boolean gate level cells and neither describes nor suggests that which is recited in the claims of the present invention, e.g., a method of designing, mapping and evaluating a new

design-specific cell at the transistor-level. This unique method of the present invention allows the design engineer to automatically optimize the size (area), signal timing, transistor sizing, number of transistors, power consumption, fault tolerance, integrity characteristics, noise characteristics, and a combination thereof at the transistor-level, which was heretofore not capable with the "NAND"/"NOR" Boolean gate level cells design and implementation system disclosed in Dangelo et al. That is, Dangelo et al. neither describes nor suggests that which is recited in the present invention of creating a unique design-specific cell at the transistor-level. Rather, Dangelo et al. utilizes pre-existing "NAND"/"NOR" Boolean gate level cells found in a standard cell library to create a system or circuit, but has no capability to create a completely new design-specific cell at the transistor-level that was not previously found in the standard cell library or to optimize the circuit at the transistor-level.

None of the specifically identified portions of the Dangelo et al, patent, i.e., col. 2, lines 38-50, col. 10, lines 43-50, col. 12, lines 57-67, col. 4, lines 11-21, col. 2, lines 31-53, col. 2, lines 1-37, col. 8, lines 65-67, col. 2, lines 38-50, and col. 11, lines 53-64, describe or suggest the designing, mapping and evaluating of a new design-specific cell at the transistor-level. Moreover, a careful review of the Dangelo et al. patent demonstrates that nowhere in that patent does it describe or suggest the creation of a design-specific cell at the transistor-level.

In summary, it is respectfully submitted for the reasons set forth above, that this amendment places the application in condition for allowance. Accordingly, it is respectfully requested that claims 1-38 be allowed and the application be passed to issue.

Respectfully Submitted,

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Paul D. Greeley, Esq.
Reg. No. 31,019
Attorney for Applicant(s)
Ohlandt, Greeley, Ruggiero & Perle, L.L.P.
One Landmark Square, 10th Floor
Stamford, CT 06901-2682
(203) 327-4500